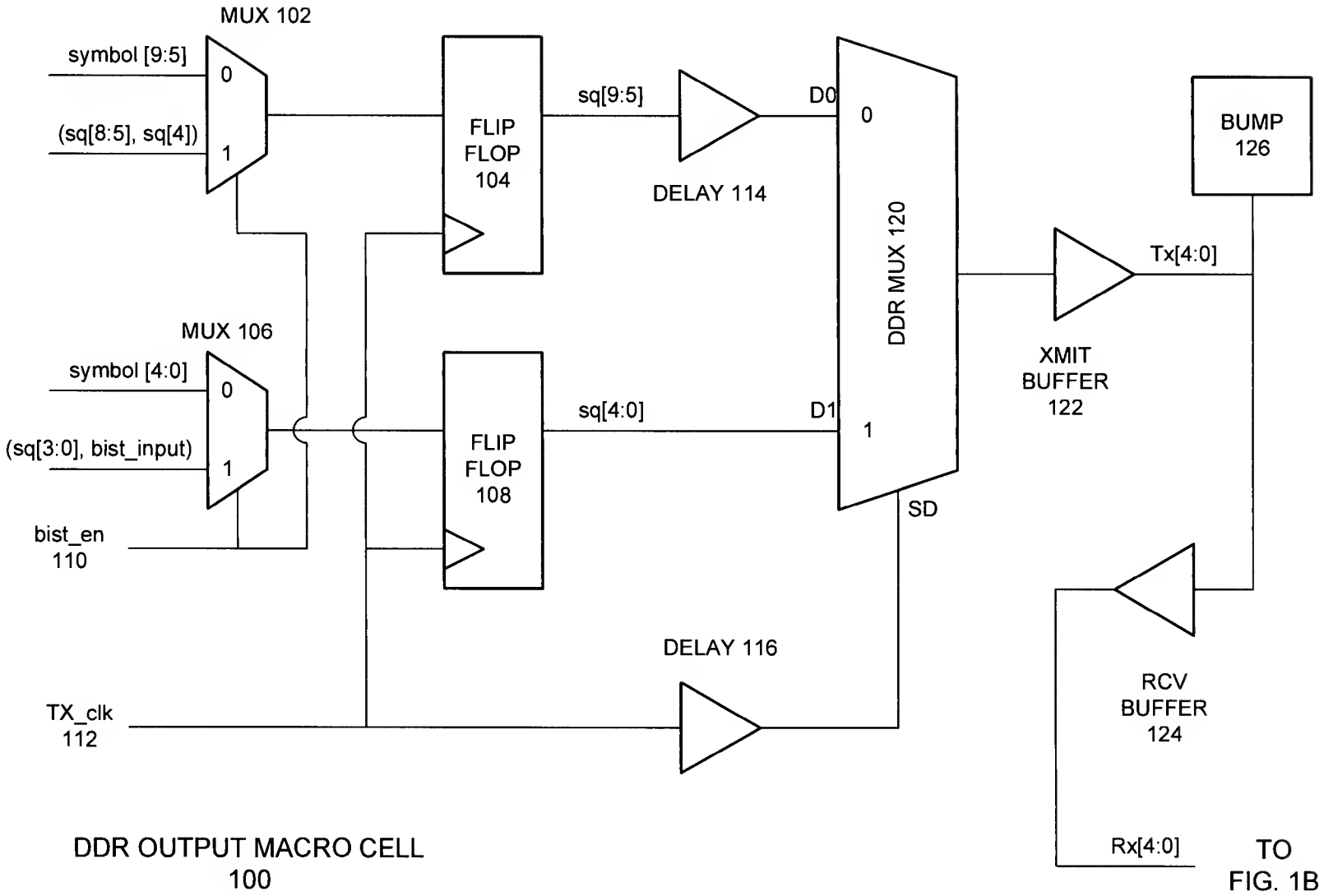
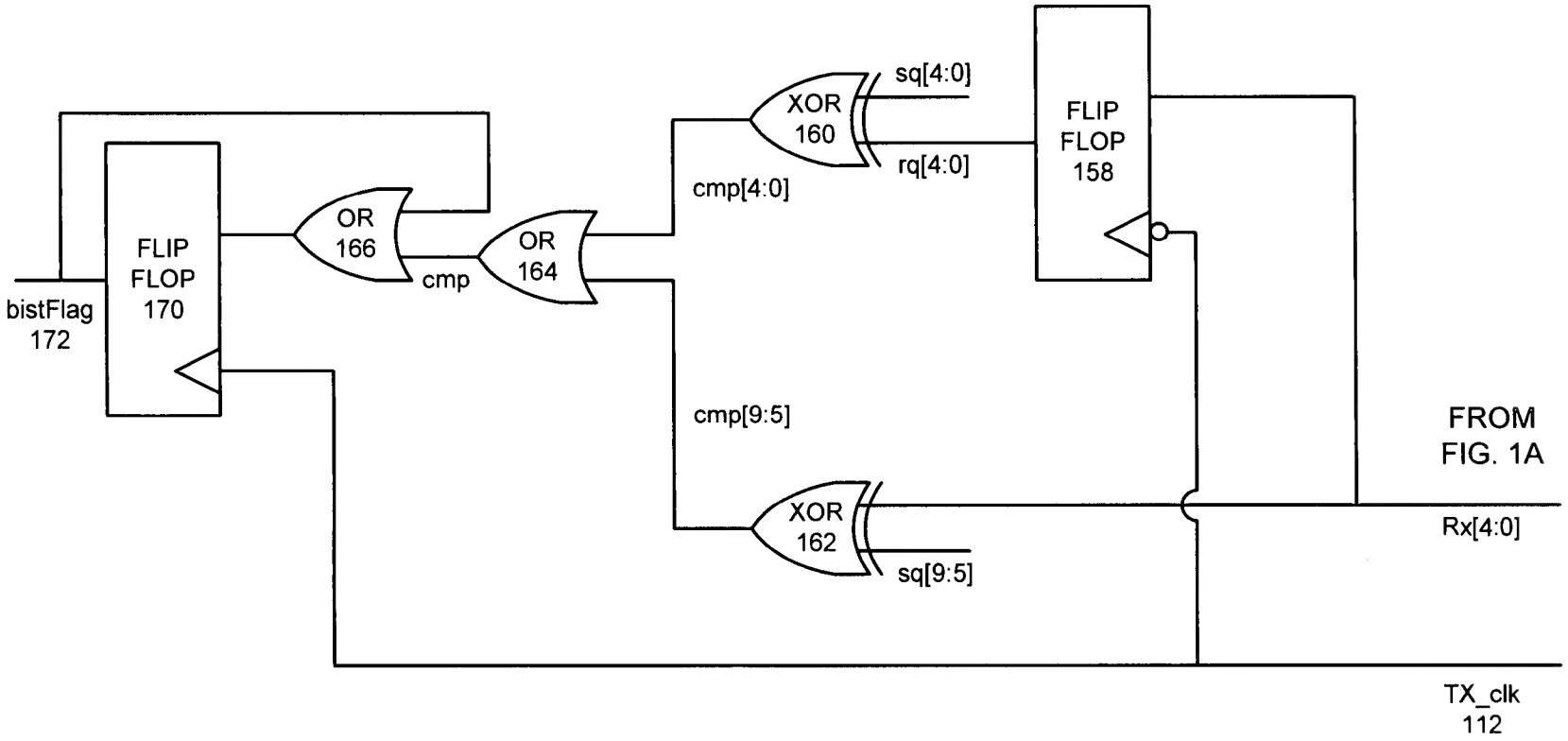
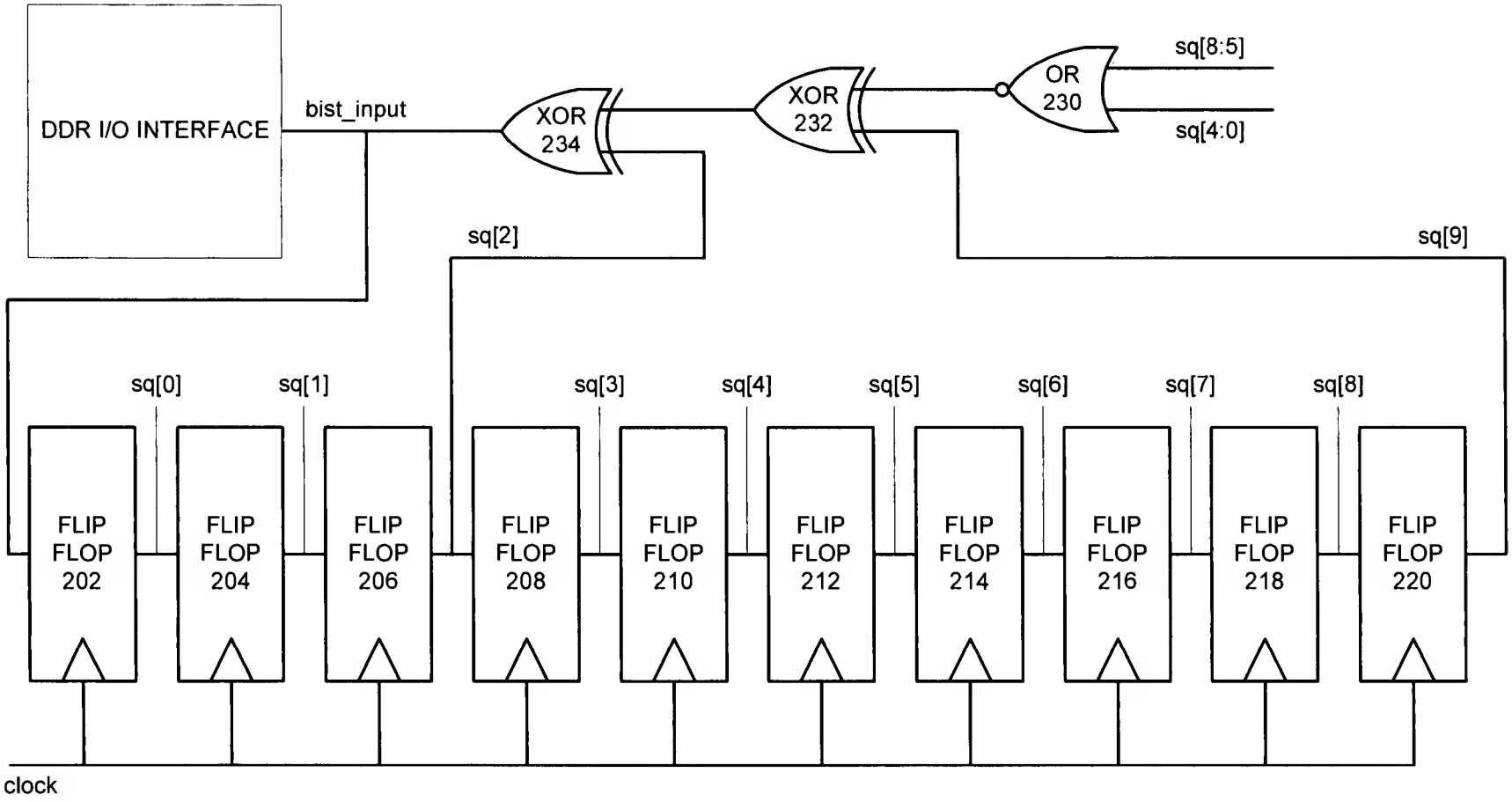

MUX 102
symbol [9:5]
(sq[8:5], sq[4])
0
1
FLIP FLOP 104
sq[9:5]
DELAY 114
D0
0
DDR MUX 120
BUMP 126
Tx[4:0]
XMIT BUFFER 122
MUX 106
symbol [4:0]
(sq[3:0], bist_input)
bist_en 110
FLIP FLOP 108
sq[4:0]
D1
1
SD
DELAY 116
TX_clk 112
RCV BUFFER 124
Rx[4:0]
TO FIG. 1B
DDR OUTPUT MACRO CELL 100

FIG. 1A



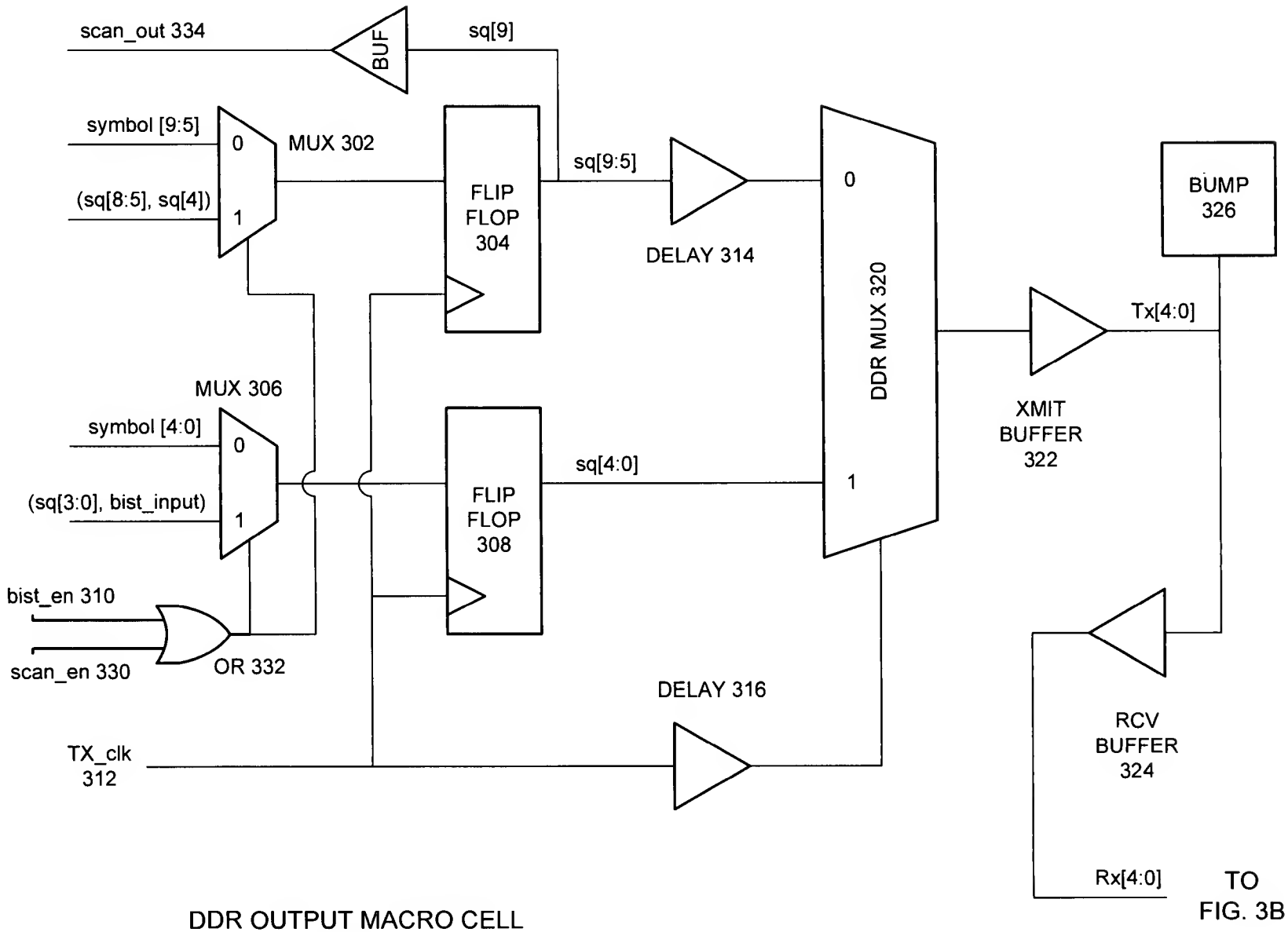
DDR OUTPUT MACRO CELL
100

FIG. 1B



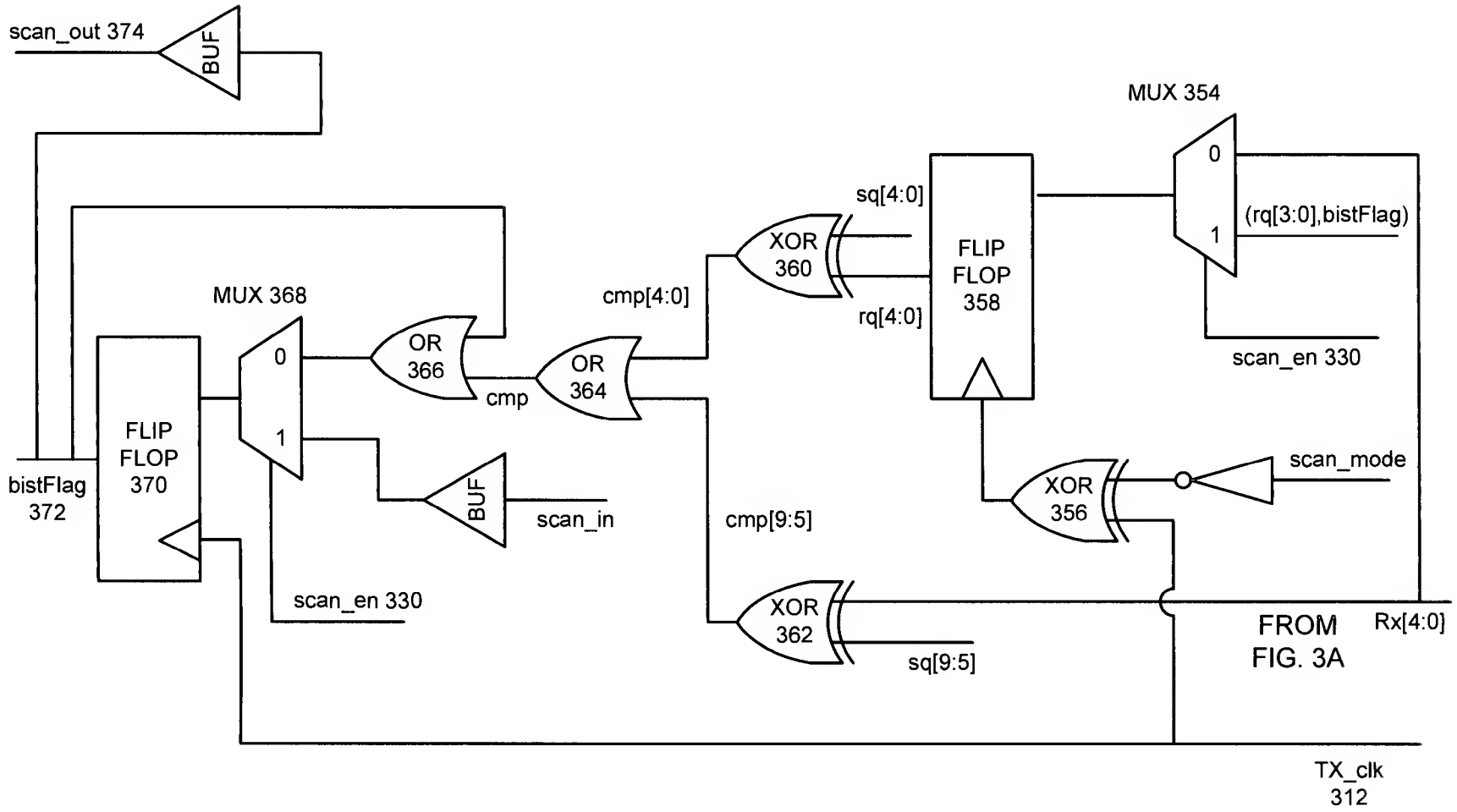
LINEAR FEEDBACK SHIFT REGISTER
200

FIG. 2



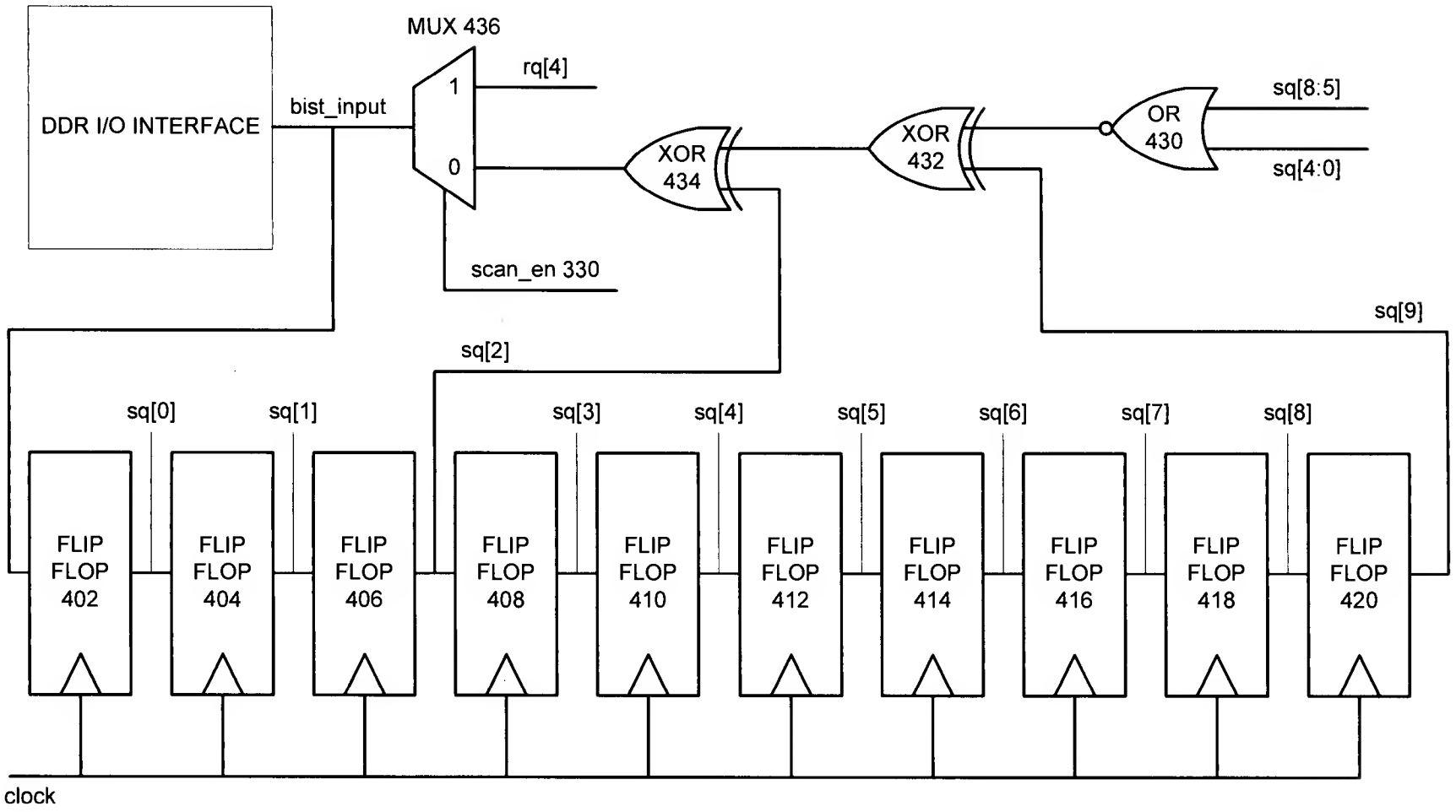
DDR OUTPUT MACRO CELL 300

FIG. 3A



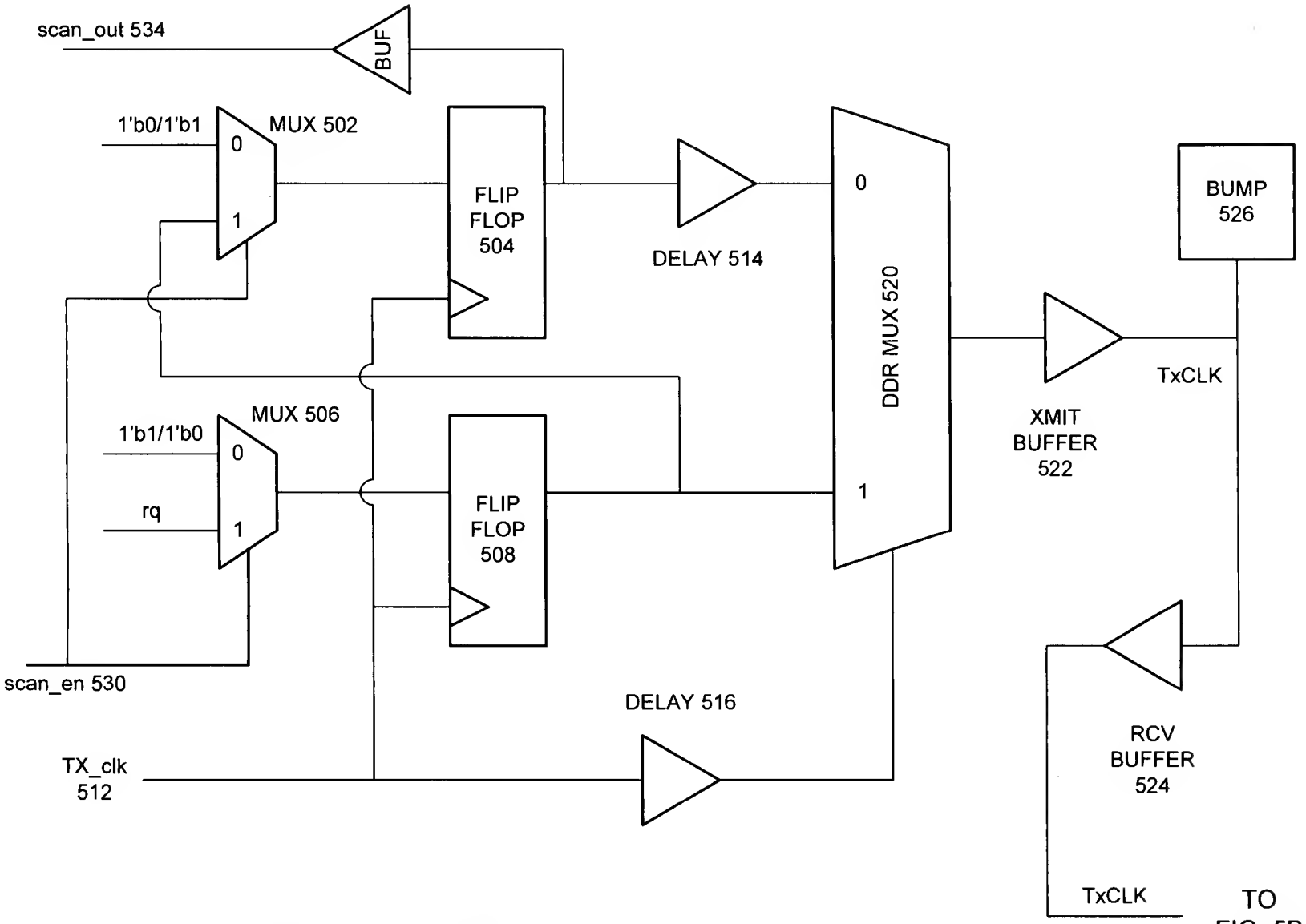
DDR OUTPUT MACRO CELL
300

FIG. 3B



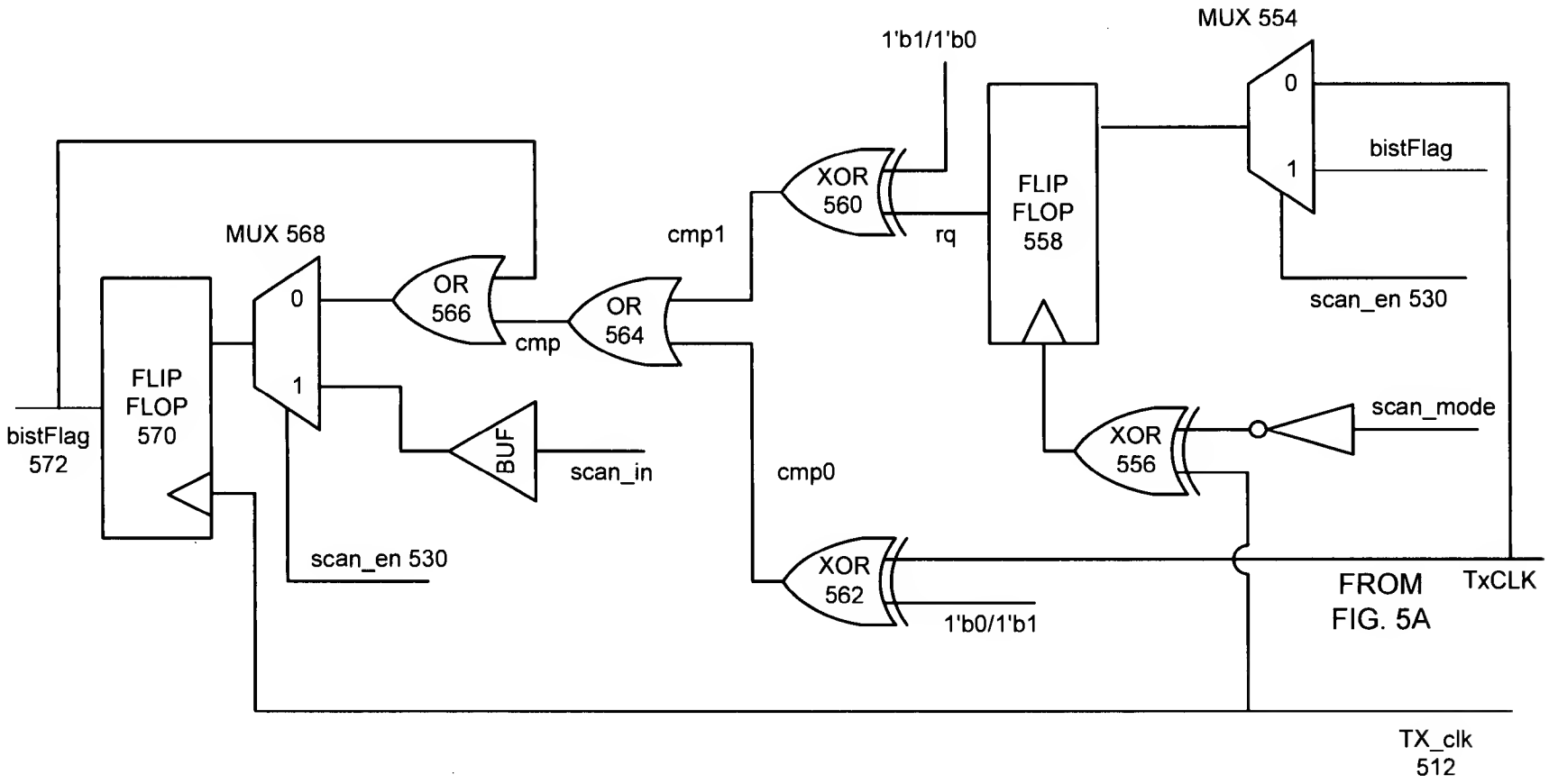
LINEAR FEEDBACK SHIFT REGISTER
400

FIG. 4



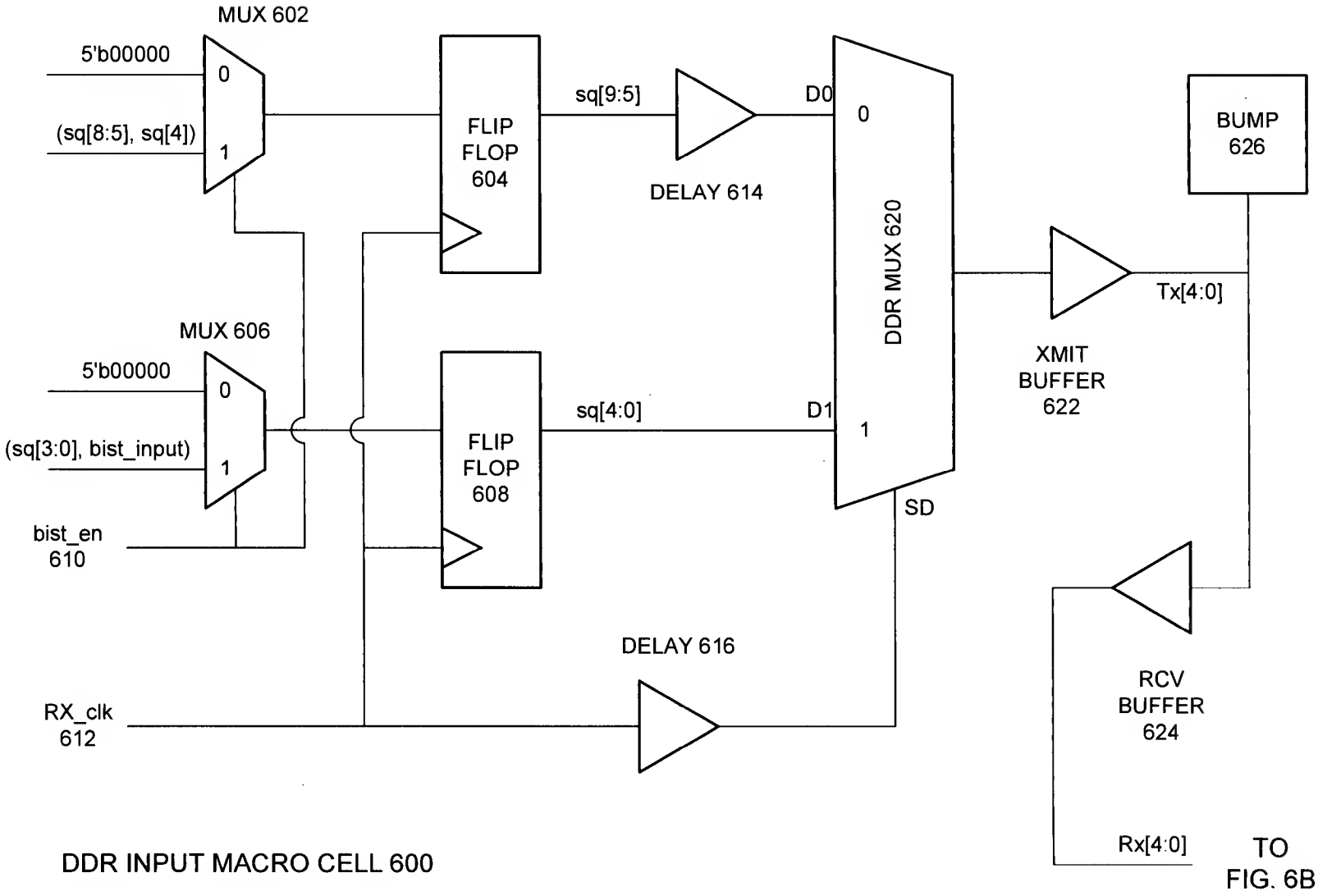
CLOCK OUTPUT MACRO
CELL 500

FIG. 5A



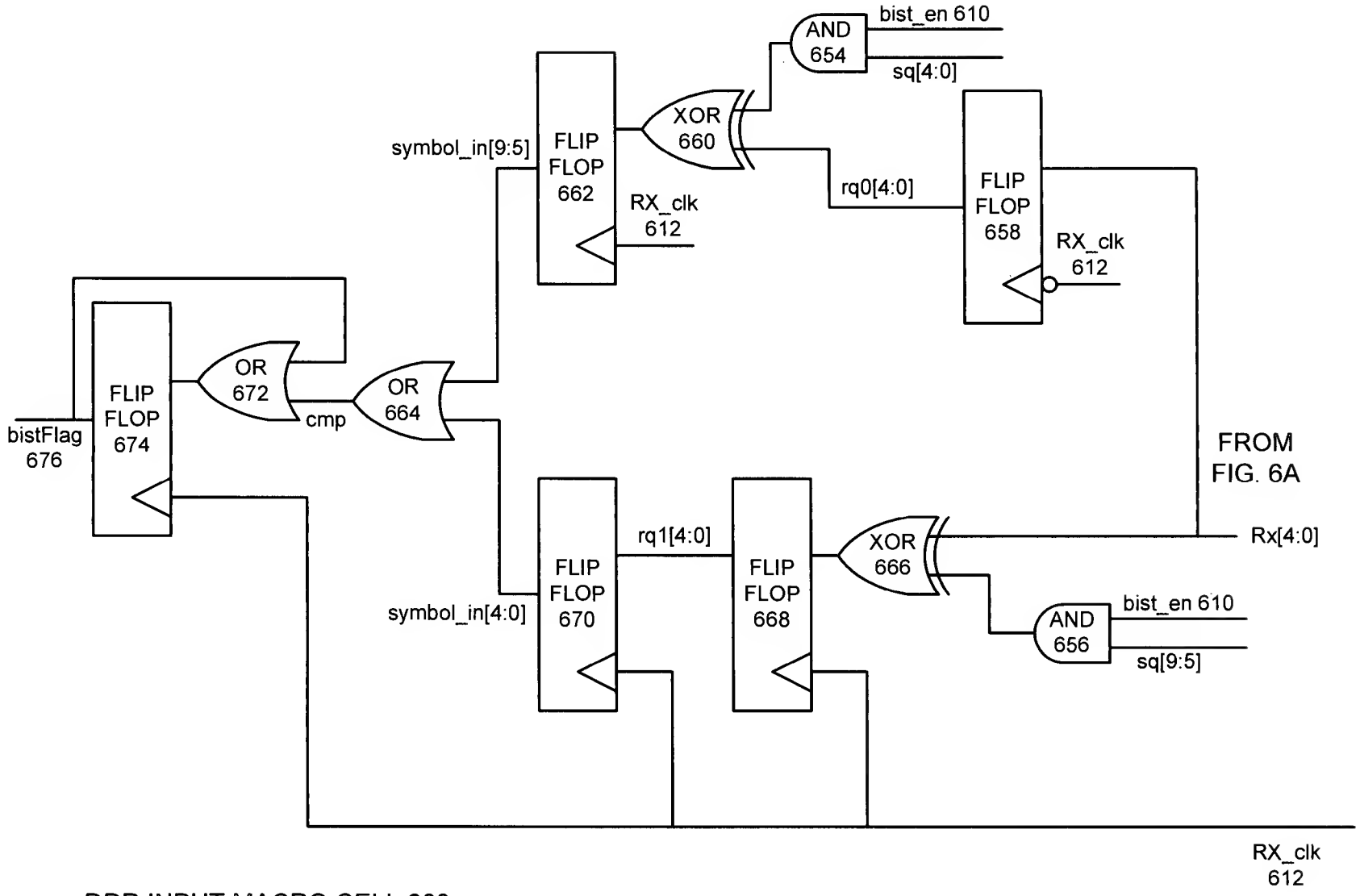
CLOCK OUTPUT MACRO
CELL 500

FIG. 5B



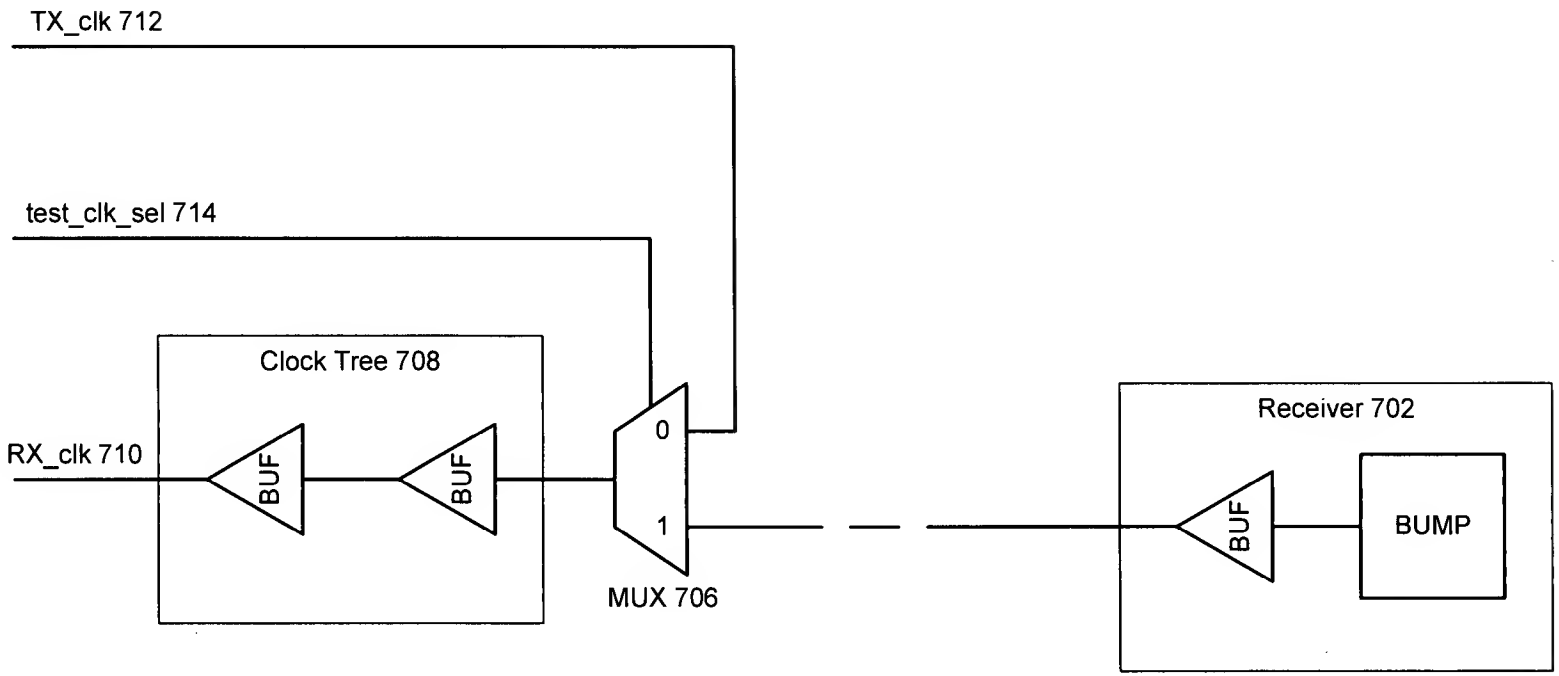
DDR INPUT MACRO CELL 600

FIG. 6A



DDR INPUT MACRO CELL 600

FIG. 6B



CLOCK INPUT MACRO CELL
700

FIG. 7

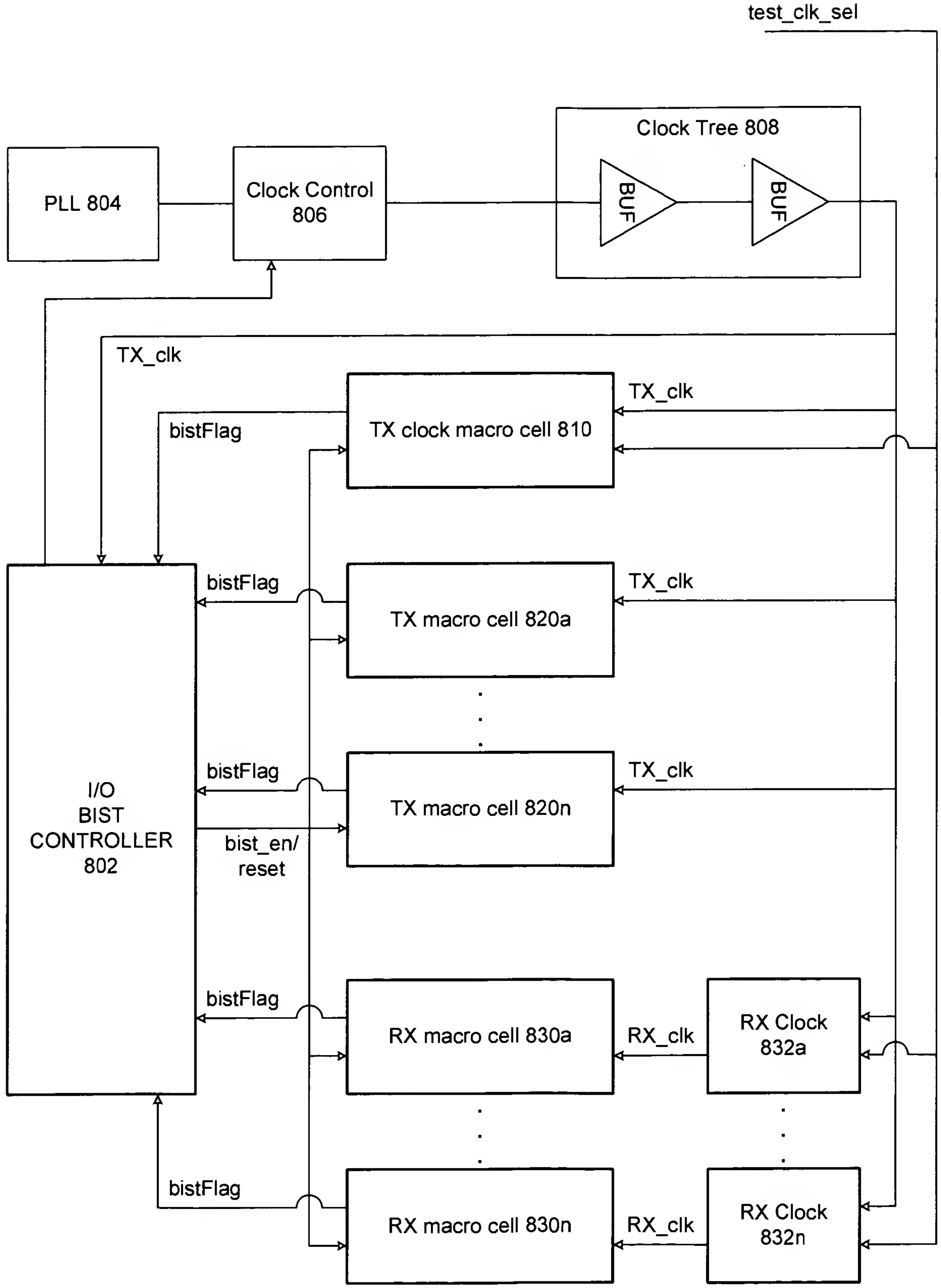


FIG. 8